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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,502	12/26/2000	Norio Yasunishi	55510(840)	4102

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EXAMINER	
DINH, DUC Q	

ART UNIT	PAPER NUMBER
2674	10

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,502	YASUNISHI ET AL.	
	Examiner	Art Unit	
	DUC Q DINH	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1,3-7,10-16,18-22 and 25-30* is/are rejected.

7)☒ Claim(s) *2,8,9,17,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 3-7, 10-16, 18-22, and 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al (US 6,320,562) in view of Yoshida et al (US 6,496,170).

As per claim 1, Ueno et al teach an STN liquid crystal display device including a plurality of row electrodes and a plurality of column electrodes 8U and 8L, a scanning voltage being applied to each of the plurality of electrodes 7, a signal voltage from the selector circuit 6 applied to each of the plurality of column electrodes, and the plurality of row electrodes intersecting the plurality of column electrodes. Further, Ueno et al teach determining, for each of the plurality of column electrodes, compensation arithmetic circuit 5 (correction data or voltage) for correcting the signal voltage based on the amount of an increase or decrease in a root-mean-square (RMS) voltage (i.e. effective voltage value) between the plurality of row and column electrodes, applying a compensation arithmetic circuit 5 (correction data or voltage) to a plurality of column electrodes 8U and 8L in accordance with the compensation arithmetic circuit 5 (correction voltage) (col. 22, lines 36-41 and 64-66, see fig. 1). Ueno et al teach two kinds of cross-talk caused by a changed in a data voltage waveform (blunt waveform) i.e. waveform caused by waveform distortion and cross-talk from distortion induced toward the side of the row

electrodes (col. 22, lines 20-24, see fig. 1). Ueno et al do not teach applying a correction voltage wherein there an increment or decrement of an effective voltage value as claimed but Yoshida et al teach a signal voltage correction circuit 79 that is set to supply a data signal voltage including the voltage decrement ΔV1R according to the formula (4) depending on a prescribed image data (col. 22, lines 57-60, fig. 7).

It would have been obvious to one of ordinary skill in the art to utilize the signal voltage correction circuit that uses voltage decrement as taught by Yoshida et al into the device of Ueno et al because it would provide a liquid crystal display apparatus capable of improving image qualities, particularly for gradational display, such as a contrast, while retaining a high-speed responsiveness at the time of effecting the display (col. 3, lines 27-31).

As per claim 3, Ueno et al teach a compensation arithmetic circuit that is determined based on a position of each of the plurality of column electrodes as claimed (see fig. 1, 5, 8U, 8L).

As per claim 4, Ueno et al teach detecting a change in the voltage applied to each of the column electrodes to be inherently a digital amount and outputting the digital amount to each of the plurality of column electrodes through the compensation circuit 5 (col. 8, lines 7-16).

As per claims 5, a method wherein an increment or decrement of the effective voltage value is an increment or decrement of an effective voltage value due to an induced distortion of the scanning voltage (col. 22, lines 19-41), and step c) further comprising the step of detecting, for each of the plurality of column electrodes, a change

in the signal voltage based on a row driver control signal, and n^{th} row display data and $(n-1)^{th}$ row display data (see fig. 1, 71, 72).

As per claim 6, Ueno et al teach detecting a change in the signal voltage for each of the plurality of column electrodes, a look-up table 52 (LUT) seen in figure 3 that does the calculation for each of the plurality of column electrodes an induced distortion correction amount based on the induced distortion count value representing the total change in the signal voltage over the plurality of column electrodes (col. 22, lines 19-41, see fig. 1, 7, 8U, 8L).

As per claim 7, Ueno et al teach a look-up table 52 (LUT) seen in figure 3 that does the calculation for each of the plurality of column electrodes an induced distortion correction amount based on the induced distortion count value and a lateral position count value representing a position of each of the plurality of column electrodes in a lateral direction as claimed along the plurality of row electrodes (col. 22, lines 19-41, see fig. 1, 7, 8U, 8L).

As per claims 10-12, a method wherein an increment or decrement of the effective voltage value is an increment or decrement of an effective voltage value due to blunt waveform of the scanning voltage and based on the signal voltage (col. 22, lines 19-41), and step c) further comprising the step of detecting, for each of the plurality of column electrodes, a change in the signal voltage based on a row driver control signal, and n^{th} row display data and $(n-1)^{th}$ row display data (see fig. 1, 71, 72).

As per claim 13, Ueno et al teach a liquid crystal display comprising a compensation arithmetic circuit 5 (correction data or voltage) capable of performing two-way gray-scale display (gradation phenomenon) including a gray-scale display by frame

based on a lateral position count value representing a position of the plurality of column electrodes along the plurality of row electrodes as claimed (col. 22, lines 9-18, see fig. 1, 7, 8U, 8L).

As per claims 14 and 15, Ueno et al teach a liquid crystal display whose gray-scale process is pulse width modulation (width and amplitude) for each compensation arithmetic circuit (correction voltage) used (col. 22, lines 12-18).

As per claim 16, it is an apparatus claim corresponding to the method claim 1 and is therefore rejected on the same basis set forth in claim 1.

As per claim 18, it is an apparatus claim corresponding to the method claim 3 and is therefore rejected on the same basis set forth in claim 3.

As per claim 19, it is an apparatus claim corresponding to the method claim 4 and is therefore rejected on the same basis set forth in claim 4.

As per claim 20, it is an apparatus claim corresponding to the method claim 5 and is therefore rejected on the same basis set forth in claim 5.

As per claim 21, it is an apparatus claim corresponding to the method claim 6 and is therefore rejected on the same basis set forth in claim 6.

As per claim 22, they are apparatus claims corresponding to the method claims 7 and 8 and are therefore rejected on the same basis set forth in claims 7 and 8.

As per claims 25-27, they are apparatus claims corresponding to the method claims 10-12 and are therefore rejected on the same basis set forth in claims 10-12.

As per claim 28, it is an apparatus claim corresponding to the method claim 13 and is therefore rejected on the same basis set forth in claim 13.

As per claim 29, it is an apparatus claim corresponding to the method claim 14 and is therefore rejected on the same basis set forth in claim 14.

As per claim 30, it is an apparatus claim corresponding to the method claim 15 and is therefore rejected on the same basis set forth in claim 15.

Allowable Subject Matter

3. Claims 2, 8, 9, 17, 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art, Ueno et al, discloses conventional liquid crystal display and a method of applying a compensation voltage for correcting the voltage applied to the column electrodes, either singularly or in combination, teaches or even suggests:

As per claim 2, a method wherein the correction voltage is applied to each of the plurality of column electrodes in a correction period, and the correction period is equal to m horizontal scanning periods is provided in L horizontal scanning periods where L is an integer greater that or equal to 2 and m is an integer more than 0 and less than L.

As per claim 8, a method wherein step d) further comprises the steps of:

calculating an induced distortion correction variable based on the lateral position count value and a frame number; and

calculating the induced distortion correction amount based on the induced distortion correction variable and the induced distortion count value.

As per claim 9, a method wherein the correction voltage is applied to each of the plurality of column electrodes in a correction period, and the correction period equal to m

horizontal scanning periods where L is an integer greater than or equal to 2 and m is an integer more than 0 and less than L, and

step a) further comprises the step of adding or subtracting an error between the correction data and the induced distortion correction amount, the correction data being applied to each of the plurality of column electrodes, to or from an induced distortion correction amount corresponding to a next correction period.

As per claim 17, a device further comprising a timing control circuit for providing a correction period, wherein the correction voltage is applied to each of the plurality of column electrodes in the correction period, and the correction period equal to m horizontal scanning periods is provided in L horizontal scanning periods where L is an integer greater than or equal to 2 and m is an integer more than 0 and less than L.

As per claim 23, a look up table for calculating an induced distortion correction variable based on the lateral position count value and a frame number; and

an induced distortion look-up table for calculating the induced distortion correction amount based on the induced distortion correction variable and the induced distortion count value.

As per claim 24, a method wherein the correction voltage is applied to each of the plurality of column electrodes in a correction period, and the correction period equal to m horizontal scanning periods where L is an integer greater than or equal to 2 and m is an integer more than 0 and less than L, and

the correction operation circuit further comprises an adding or subtracting an error between the correction data and the induced distortion correction amount, the correction

data being applied to each of the plurality of column electrodes, to or from an induced distortion correction amount corresponding to a next correction period.

Response to Arguments

4. Applicant's arguments pages 18-21, filed 6/4/04 have been fully considered but they are not persuasive. Applicant argues Ueno et al. reference teaches the calculation of a single correction value which is thereafter applied to tall of the column electrodes... However, Ueno et al. teaches "liquid crystal display device includes: a compensation circuit for generating a compensation data signal for compensating for a change in a RMS value caused by a waveform change of a voltage applied to one of the plurality of column electrodes; and a driving circuit for applying the display data voltage and a compensation voltage based on the compensation data signal to one of the plurality of column electrodes during one frame period. As a result, a RMS value which increases or decreases according to the waveform change of the voltage applied to one of the column electrodes can be compensated. Therefore, the rejection is maintained.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **DUC Q DINH** whose telephone number is **(703) 306-5412** The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD A HJERPE** can be reached on **(703) 305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivery response should be brought to: Crystal Park II, 2121 Crystal Drive, Arlington, Va Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

DUC Q DINH
Examiner
Art Unit 2674

REGINA LIANG
PRIMARY EXAMINER